AMENDMENTS TO THE CLAIMS

Please amend Claims 10-15 and 17-18 as indicated in the listing of claims below:

1. (Previously presented) A display system, comprising:

a standardized display driver to provide address voltages;

an array of interferometric elements; and

a voltage adjuster to adjust address voltages to provide adjusted row address voltages to the array of interferometric elements,

wherein the voltage adjuster further comprises a resistor divider network configured to lower the address voltage amplitudes that are provided by the standardized display driver.

2. (Original) The display system of claim 1, the standardized display driver further comprising a driver for a liquid crystal display.

3. (Previously presented) The display system of claim 1, the may of interferometric elements further comprising an array of iMoD™ elements.

4. (Canceled)

5. (Original) The display system of claim 1, the voltage adjuster to adjust row address voltages.

6. (Original) The display system of claim 1, the voltage adjuster to adjust column address voltages.

7. (Previously presented) A method of manufacturing an array of modulator elements and an adjuster circuit, comprising:

depositing a first metal layer on a transparent substrate;

patterning and etching the first metal layer to form electrodes;

depositing an optical stack layer;

depositing a first sacrificial layer upon the optical stack layer;

depositing a second metal layer on the sacrificial layer;

patterning and forming the second metal layer to form modulator elements;

forming a resistor divider network configured to lower address voltage amplitude that are provided from a standardized display driver; and

forming resistors from one metal layer and connecting the resistors with a subsequent metal layer.

8. (Original) The method of claim 7, forming the resistors from one metal layer further comprising forming the resistors from the first metal layer and connecting the resistors with the second metal layer.

9. (Original) The method of claim 7, further comprising:

depositing a second sacrificial layer;

depositing a third metal layer on the second sacrificial layer; and

patterning and etching the third metal layer to form posts and supports.

10. (Currently amended) The method of claim 7 ~~20~~, forming the resistors further comprising forming the resistors from the first metal layer and connecting the resistors using the third metal layer.

11. (Currently amended) The method of claim 7 ~~20~~ forming the resistors further comprising forming the resistors from the second metal layer and connecting the resistors using the third metal layer.

12. (Currently amended) The method of claim 7 ~~20~~, further comprising:

depositing a third sacrificial layer;

depositing a fourth metal layer on the third sacrificial layer;

patterning and etching the fourth metal layer to form a bus layer.

13. (Currently amended) The method of claim 7 ~~20~~, forming the resistors from one metal layer further comprising forming the resistors from the first metal layer and connecting the resistors using the fourth metal layer.

14. (Currently amended) The method of claim 7 ~~20~~, forming the resistors from one metal layer further comprising forming the resistors from the second metal layer and connecting the resistors using the fourth metal layer.

15. (Currently amended) The method of claim 7 ~~20~~, forming the resistors from one metal layer further comprising forming the resistors from the third metal layer and connecting the resistors using the fourth metal layer .

16. (Previously presented) A resistor network, comprising:

an incoming address line;

a first resistor connected between the address line and a conductive bus; and

a second resistor connected between the address line and an adjusted address line, wherein the resistor network lowers address voltage amplitudes provided by a standardized display driver.

17. (Currently amended) The resistor network of claim 16 ~~13~~ the address line further comprising a row address line.

18. (Currently amended) The resistor network of claim 16 ~~13~~, the address line further comprising a column address line.

19. (Previously presented) The method of manufacturing of Claim 7, wherein the resistor divider network is formed on the same substrate of the array.

20. (Previously presented) The method of manufacturing of Claim 7, wherein the resistor divider network is formed on the first metal layer.

21. (Previously presented) The method of manufacturing of Claim 7, wherein the resistor divider network is formed on the second metal layer.